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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,532	11/03/2003	Takuya Kobayashi	61282-043	1414

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EXAMINER	
NGUYEN, STEVE N	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,532	KOBAYASHI, TAKUYA	
	Examiner	Art Unit	
	Steve Nguyen	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *1-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 are currently pending.

Claim Rejections - 35 USC § 112

2. The U.S.C. 112, second paragraph rejection of claims 1, 2, 7, and 8 has been withdrawn in view of the amended claims.

Response to Arguments

3. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

Specification

4. The abstract of the disclosure is objected to because the last line refers to a drawing and should be deleted. Correction is required. See MPEP § 608.01(b).

Claim Objections

5. Claims 1 and 7 objected to because of the following informalities: the first limitation should begin: "a first and a second flip-flop". The forth limitation recites, "comparing the output from said third flip-flop and the expected value". This should be corrected to "an expected value" since there is no antecedent basis for "the expected

value". The sixth limitation recites, "compared with an expected value". This should be corrected to "the expected value" to correlate with the aforementioned expected value. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1, 3, 5, and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie et al (US Pat. 5,349,587; hereinafter referred to as Dostie).

As per claims 1 and 7:

Dostie teaches a path delay measuring circuitry for judging a signal transition time of a combination circuit whose path delay is to be measured, comprising:

- a first and a second flip-flop which are connected to an input of the combination circuit and constitute a scan-chain (col. 4, lines 13-17; see Fig. 2, in which a flip-

flop of a scan cell is connected to input 51 through multiplexer 54. A second flip-flop connected to the output of the first is not explicitly shown, but it would be clear to one of ordinary skill in the art that the scan chain 50 is simplified and that many flip-flop scan cells would have been used);

- a third flip-flop which is connected to an output from said combination circuit to constitute the scan chain (Fig. 2, a scan cell in the scan chain 50 is connected to output 52);
- a pattern creating circuit for creating a test pattern to be set for said first and said second flip-flop (col. 5, lines 34-35);
- a comparison/decision circuit for comparing the output from said third flip-flop and the expected value (col. 5, lines 35-36); and
- a timing signal creating circuit for supplying an operation timing signal to each of the first, second and third flop-flops (col. 5, lines 33-34),
- wherein after a test pattern is set for said first and said second flip-flop by a shifting operation of the scan chain (col. 4, lines 35-37), the output from said combination circuit is taken into said third flip-flop by a capturing operation (col. 4, lines 45-47; see Fig. 3 which shows the output SO of the last flip-flop being provided to the test response processor 64 for comparison) and an output from said third flip-flop is compared with an expected value (col. 4, lines 47-50), and
- wherein said first flip-flop, said second flip-flop and third flip-flop are each clocked utilizing the same clock signal (col. 5, lines 41-45).

Not explicitly disclosed by Dostie is supplying an operation timing signal to said pattern creating circuit and said comparison/decision circuit. However, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide clock signals to the other elements in the system. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the logic elements of Dostie all require a clock signal because they operate synchronously with the scan chains in the test mode.

As per claim 3:

Dostie further teaches a path delay measuring circuitry according to claim 1, wherein a plurality of flip-flops are provided which are identical to said first and second flip-flops (col. 3, lines 60-63).

As per claim 5:

Dostie further teaches a path delay measuring circuitry according to claim 1, wherein a plurality of flip-flops are provided which are identical to said third flip-flop (col. 3, lines 60-63).

7. Claims 2, 4, 6, and 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Dostie in view of Chao et al (US Pat. 6,671,847; hereinafter referred to as Chao).

As per claims 2 and 8:

Dostie further teaches a path delay measuring circuitry, further comprising:

- a multiplying circuit for creating a high speed clock on the basis of a clock externally supplied (col. 6, lines 8-12);
- a clock mode counter for outputting a clock mode value which is updated whenever said signal transition time is decided (col. 5, lines 62-65; a clock mode value is provided as standard protocol by the TAP).

Not explicitly disclosed by Dostie is a clock creating circuit for creating another clock to be supplied to said path delay measuring circuit on the basis of said high speed clock and said clock mode value; and wherein the clock created by said clock creating circuit is made variable.

However, Chao in an analogous art teaches a clock generator for creating a clock on the basis of a core clock which can be made variable (col. 6, lines 11-16). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the clock of Chao in the system of Dostie. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have been motivated to do so in order to be able to test timing parameters in the circuit as disclosed by Chao (col. 2, lines 44-49).

As per claim 4:

Dostie further teaches a path delay measuring circuitry according to claim 2, wherein a plurality of flip-flops are provided which are identical to said first and second flip-flops (col. 3, lines 60-63).

As per claim 6:

Dostie further teaches a path delay measuring circuitry according claim 2, wherein a plurality of flip-flops are provided which are identical to said third flip-flop (col. 3, lines 60-63).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steve Nguyen whose telephone number is (571) 272-7214. The examiner can normally be reached on M-F, 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Examiner
Art Unit 2138

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